REMARKS

Favorable reconsideration of this application is requested in view of the foregoing amendments and the following remarks. Claims 1-6, 15, and 27 are pending in this application. Claims 7-14, 16-26, 28-30 and 31-48 were previously canceled without prejudice or disclaimer.

The claims are amended in order to more clearly define the invention, support for which is found in the figures and related parts of the specification. Specifically, support for the recitation in independent claims 1 and 27 of wherein a main clock phase lock loop is allowed to adjust without the phase build-out activity occurring when the skip timer is loaded and a frequency offset signal is asserted is found at page 15, lines 1-3 and 9-14 of the specification (and fig. 6) as originally filed.

Claims 1-6, 15 and 27 stand rejected under 35 USC 102(b) as anticipated by Jones et al. (i.e., U.S. Pat. No. 6,078,595, hereinafter Jones). Claims 1 and 27 are amended to specify that a main clock phase lock loop is allowed to adjust without the phase build-out activity occurring when the skip timer is loaded and a frequency offset signal is asserted.

As pointed out in the Office Action at page 3, Jones not does perform jitter attenuation when the Jones clock signal is in inactive mode. The claimed limitation of allowing the main clock phase lock loop to adjust without phase build-out activity occurring has the practical effect of supporting jitter attenuation continually on both the primary and secondary inputs. Thus, Jones teaches away from the claimed invention. It can be appreciated that the claimed invention solves the problem of switching references with minimal outage time since continuing to adjust without the phase build-out activity occurring reduces the amount of time needed for the line interface unit to settle on the new reference.

Incidentally, at page 2, the Office Action states that the Jones reference discloses "...receiving a pair of input clock signals (SYSCLK1 and SYSCLK2, col. 4, lines 18-24)...."

However, referring to column 4, lines 18-24 of Jones, SYSCLK1 and SYSCLK2 of Jones are outputs and not inputs.

Accordingly, withdrawal of this rejection is respectfully requested.

Other than as explicitly set forth above, this reply does not include acquiescence to statements, assertions, assumptions, conclusions, or any combination thereof in the Office Action. In view of the above, all the claims are considered patentable and allowance of all the claims is respectfully requested. The Examiner is invited to telephone the undersigned (at direct line 512-394-0118) for prompt action in the event any issues remain that prevent the allowance of any pending claims.

In accordance with 37 CFR 1.136(a) pertaining to patent application processing fees, Applicant requests an extension of time from March 21, 2005 to May 21, 2005 in which to respond to the Office Action dated December 21, 2004. A notification of extension of time is filed herewith.

The Director of the U.S. Patent and Trademark Office is hereby authorized to charge any fees or credit any overpayments to Deposit Account No. 50-3204 of John Bruckner PC.

Respectfully submitted,

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Dated: May 21, 2005

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